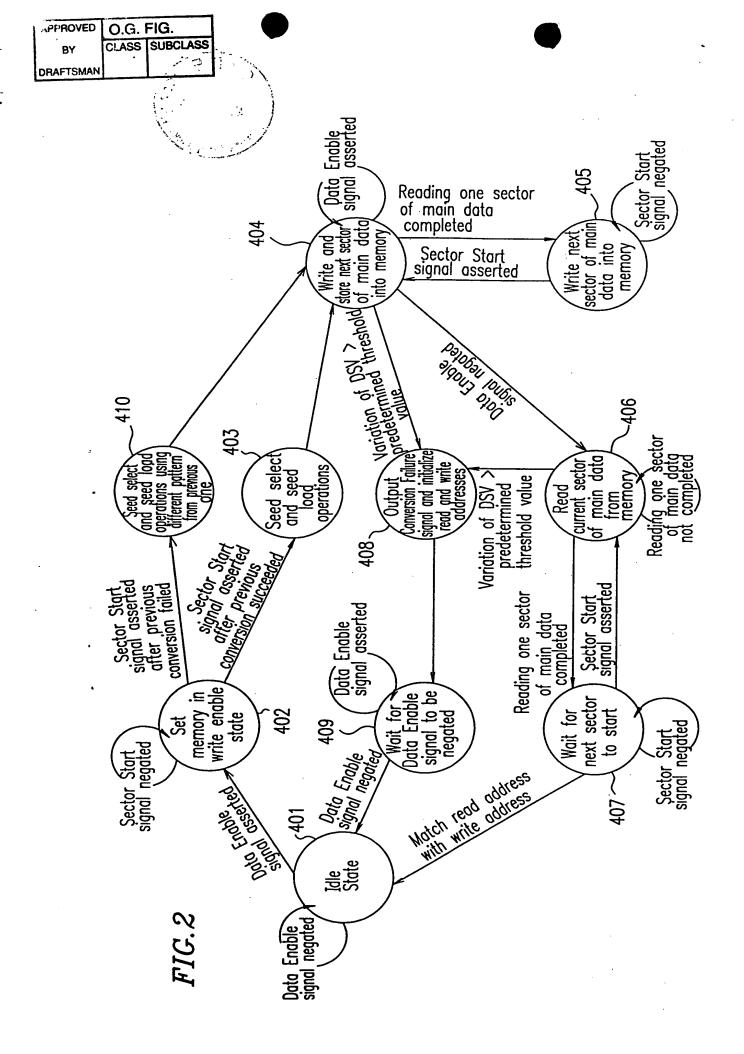
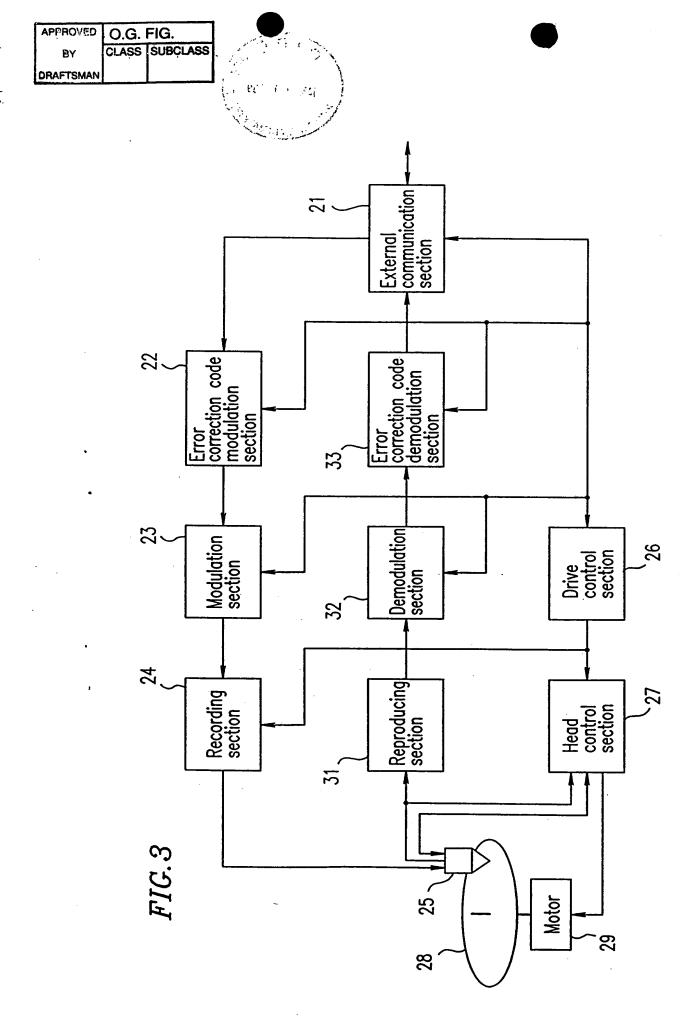
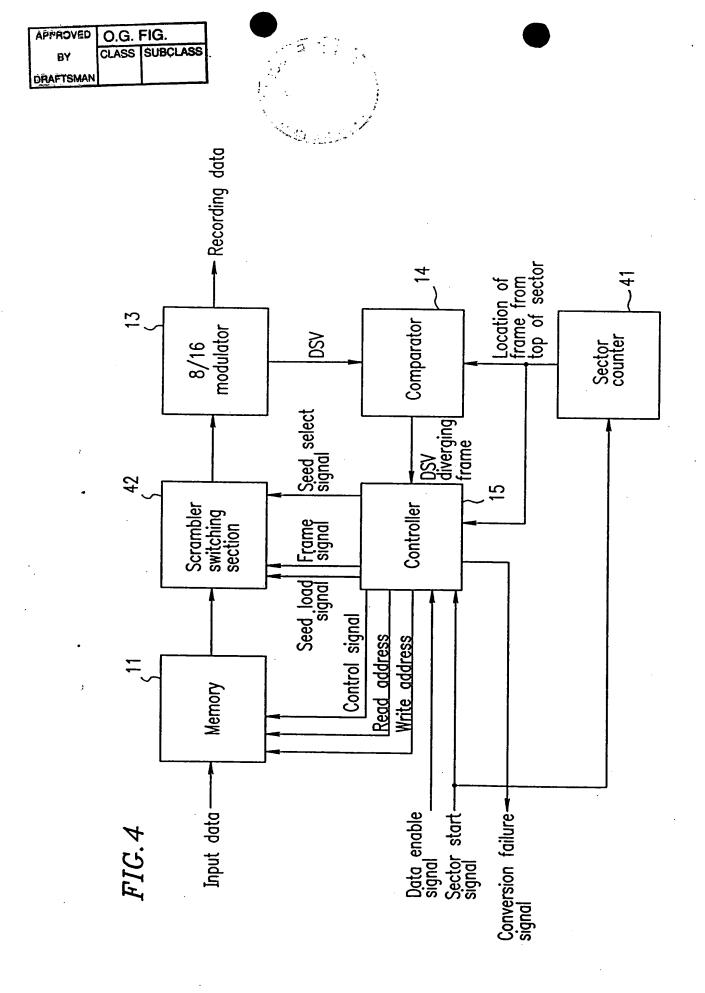


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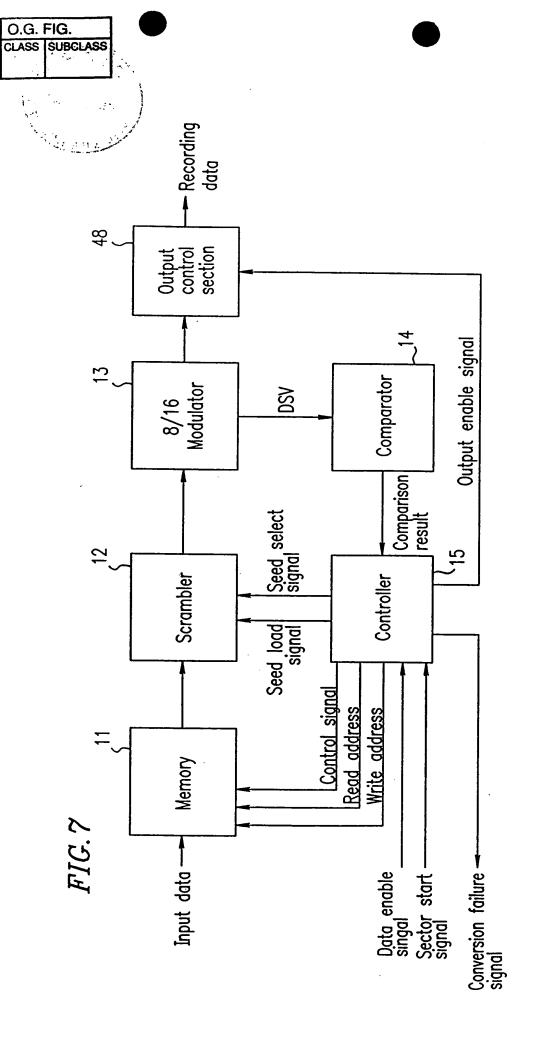






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\ \ F	Bit clock— Word clock— Reset signal—	Gate signal on a frame basis Input data—

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				•			/"	Write next sector of main	智智人	Sector Start signal negated
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						e sector peted ada completed ada signal as and divergin	200 3	neuviling one section for main data completed	Sector Start signal asserted in DSV diverging frame	
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				504	Regalling	int signification	<i>y"</i>	5-8 275	5.E	
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		. <b>.</b>	signal asserted	White and next sector late into more sector late into more sector late more sector late into more sector late late late late late late late late	<b>WODSY</b>	diverging fra	me 7	White and next sectorate into m	<b>F</b>	Endb ass
ç			1	Write and store next sector of main data into memory, frame signal	ngv.	on_diversing	frama	Write and store of store next sector of main data into memory.	Frame signal asserted	Data Enable signal asserted
				1 Sile	/ 1311	non—diverging	Hulle	AS.E	<u> </u>	
•			DS non-divening terms	rration of USV > predetermined   threshold value	Yara /	ging frame	te Te		51	
	~			Variation of USV  > predetermined threshold value threshold va	VON OUR	Sec	det	956		
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	)	510	\$/		Sold and Sol		completed not	Data Enable signal negated	ر 512	pat
					= /	是	< viragii	9/富二	<b>∠</b> ′′ .	Keading one Sector of main data non-completed
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. \	Seed select and	Seed gode gode seed select	and seed logd operations using different pattern from previous	Conversion failure signed or		Read current sector of main da from memory, frame sonal		Read current Sector of man d	Frame signal asserted	
•	<b>₹</b> 1	ノ			Variation of DSV : predetermin threshold v				7	<u>秦</u> -튙
	433		_† -	20%	predetermin	ed \\	frame	<b>&amp;</b>	<u> </u>	Ö
•					threshold v	olue		25 E	9 S E	
	chat simila asserted	Sector Start signal Sector Start signal asserted after previous	是 是 是 是			due particular particu	non-diverce frame	signal asserted of diverging frame	Reading one sector of main data completed	
	Ü	Sector (18) Sector	Signal asserted	$\bigcap$	203	180 E		<b>S</b>	2 E	
		3 1						¥.≡	7	
	c	v	e 를 실 /				Spill	्रहेव्	E /	Sfart
		700	in write enable state		Oola Enable	<u></u>	**************************************	Wait for next sector		Sector Start signal negated
			ا ا	Wait for Data Enable signal to be	Dala Enable signal negaled	`름 은		入	~	-W.W
	6	Seat Seat Seat Seat Seat Seat Seat Seat	· · ·		<u> </u>	<b>~</b> ~暑·景	moy emply	,	507	
	$\mathcal{C}$	Sector Start— signal negated	Signa	to Enoble coserled	state	W.	mory C.		4,	
	FIG. 6	<b>3.5</b>		<i>क्रमास</i> ट्रि		1 "				
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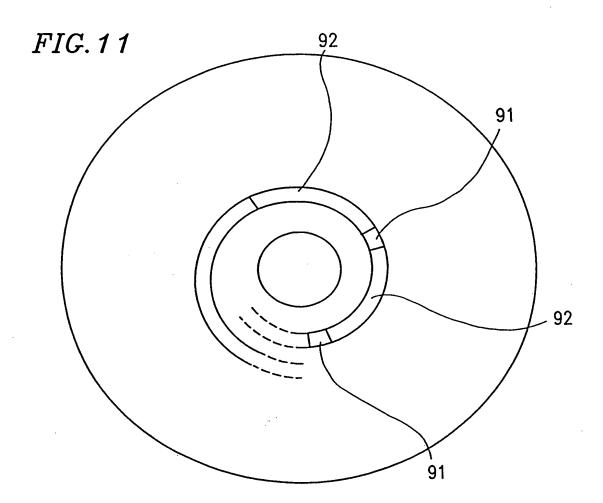
EDC <del>4</del>B MAIN DATA(Do  $\sim D_{159}$ ) MAIN DATA(D1708 ~ D1879) MAIN DATA( $D_{1880} \sim D_{2047}$ ) MAIN DATA(D160~D331) SCL **6B** 田 28 DATA ID FIG.812 ROWS

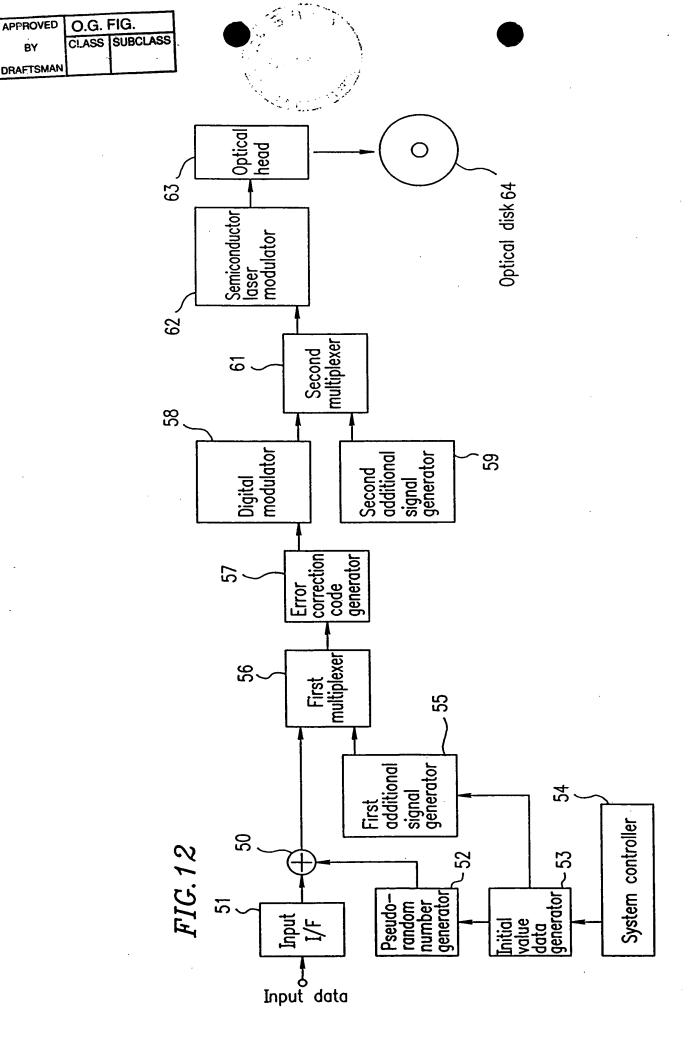
MARINAM RIEN	U.G. 1		:
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O.G. FIG. CLASS SUBCLASS APPROVED · BY DRAFTSMAN Sync frame 918 SY5 SY5 SY6 SY5 SY5 SY5 SY6 SY6 SY6 SX SY7 SX7 SX1 28 Sync frame 918 SY2 SY3 SY4 SY2 SX3SY4 SY3 SY4 S<del>₹</del> **S**₹1 SY2 SZ. 28 FIG. 10

13 ROWS

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FIG. 13

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FIG. 14

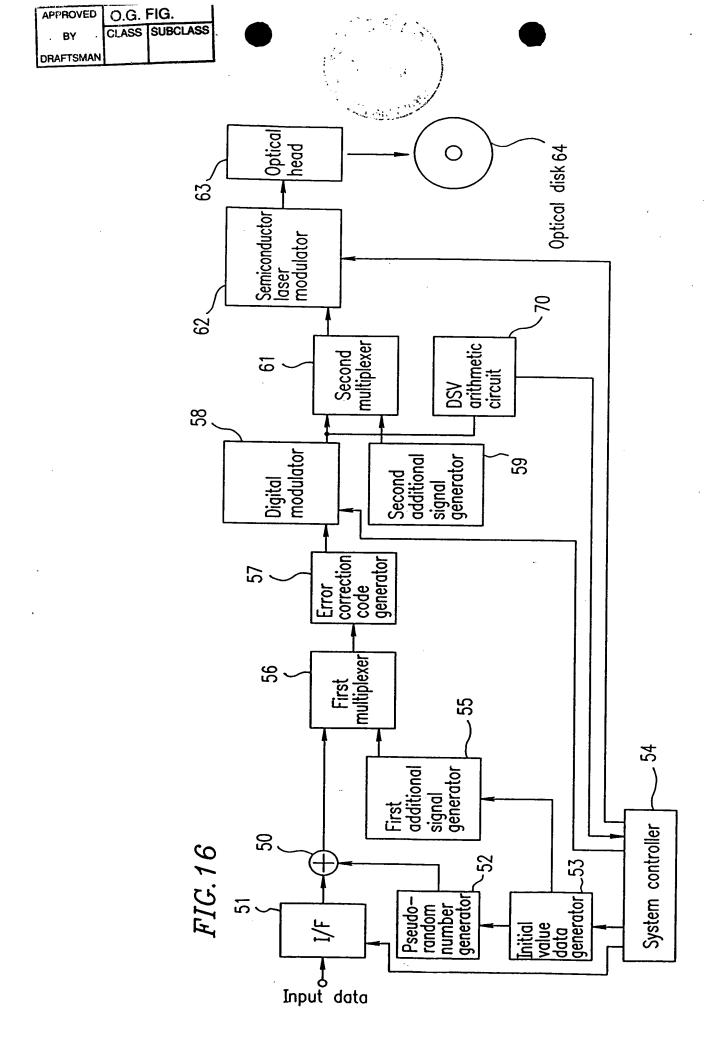
Bit string	Initial value
0h	0001h
1	5500
2	0002
3	2A00
4	0004
5	5400
6	0008
7	2800
8	0010
9	5000
Α	0020
В	2001
С	0040
D	4002
E	0800
F	0005

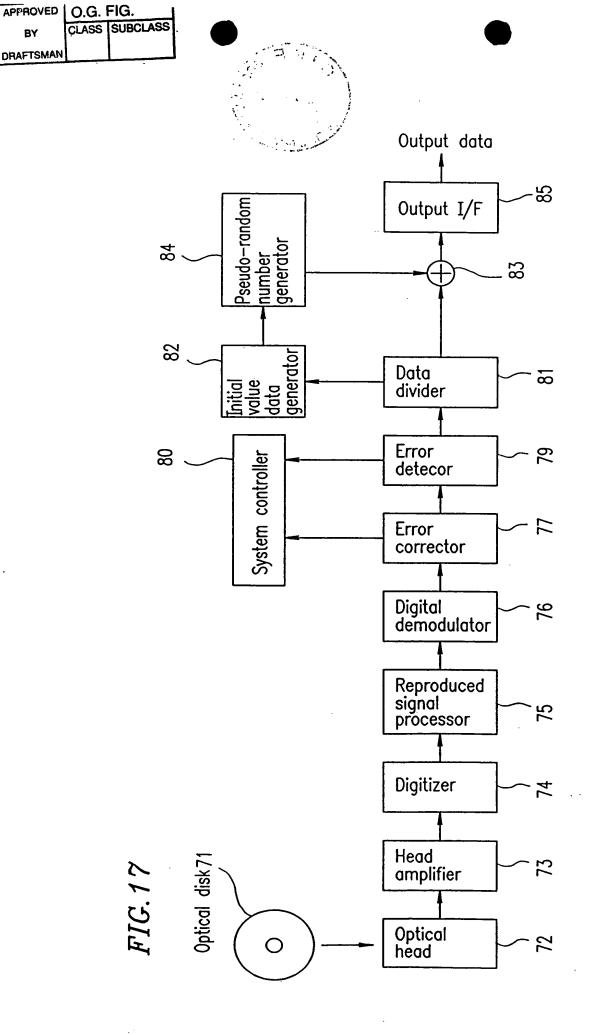
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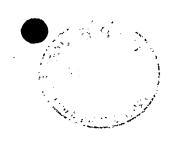
					,											
Rewrite repetition times 15	0031h	2000	0032	1600	0034	2800	0038	1300	0013	2A00	0023	2007	0043	400E	0083	00A2
1		1			1				1	  -  -  -  -  -			 			1
Rewrite repetition times 2	0003h	2400	2000	1200	9000	2300	2000	1100	0030	2500	0020	3001	0900	6002	0020	0052
Rewrite repetition times 1	40600	3C00	00A0	1E00	0000	3800	00F0	1000	6000	3A00	000A	1003	0000	2006	000F	00A3
Initial Rewrite repetition Rewrite repetition Rewrite repetition times 2	0001h	2500	2000	2A00	4000	5400	8000	2800	0010	2000	0020	2001	0040	4002	0080	0002
Bit Initial String	Oh	1	2	3	4	5	9	7	8	6	A	В	၁	O	L	L

FIG. 15



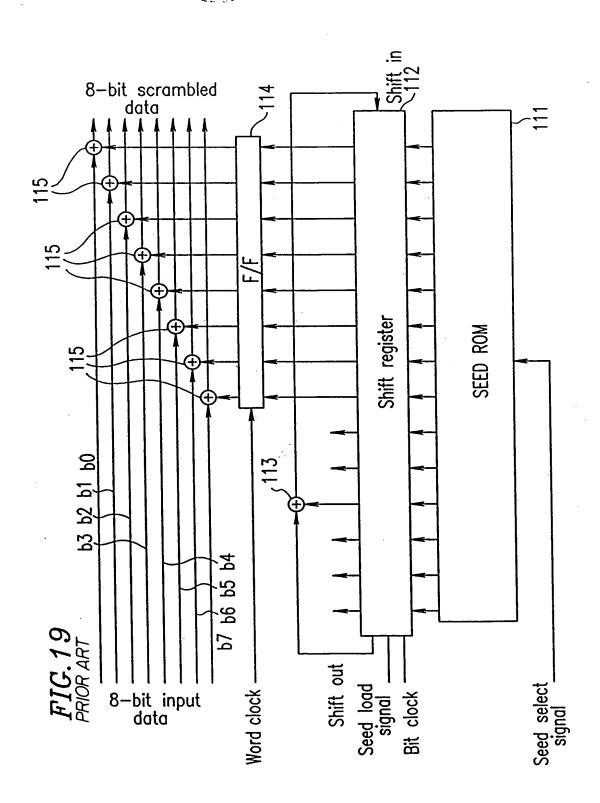


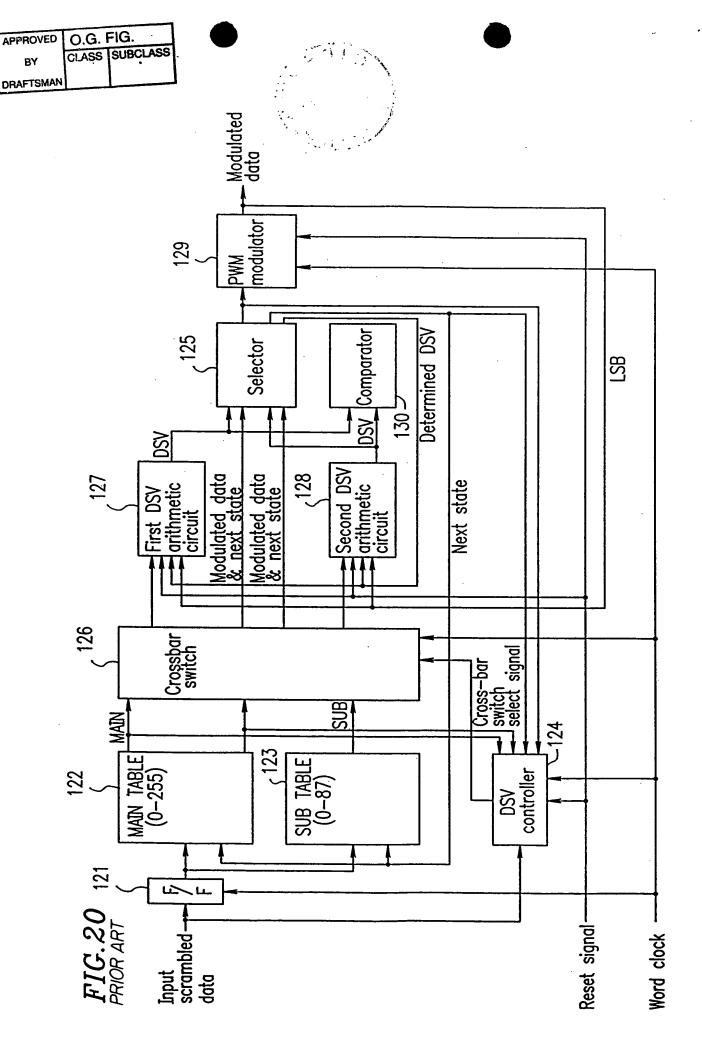
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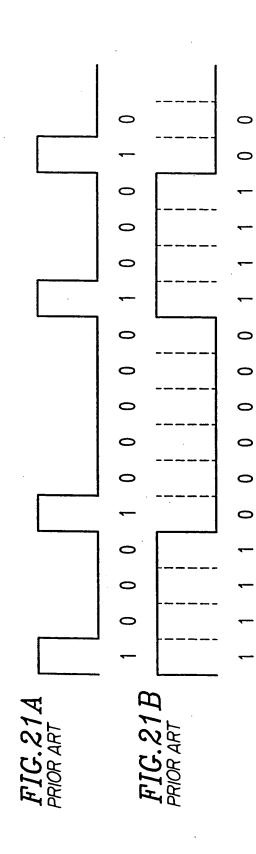
- Recording data 8/16 modulator Scrambler Input data— Bit4 to bit7 of logical address Sector start signal -FIG.18

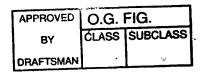
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APPROVED	O.G. FIG.	
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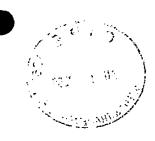


FIG. 22 PRIOR ART

